PhD proposal

« Simplified non-binary decoders »

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Key words: IoT, communication, hardware/software implementation, algorithm design, error control code.

PhD period: October 2023-September 2026

Abstract: In the QCSP project, UBS and IMS have developed a hardware solution for a real-time reception of short fame called “Quasi-Cyclic Short Packet (QCSP)”. This project led to studies and measurement campaign in several communication channel: mobile channel, sea buoy-boat and IoT sensor-Low Earth Satellite.

For the moment, only the detection and synchronization aspects have been implemented. The non-binary decoder constituting the outer code of a QCSP frame remains a blocking point for low cost receiver because of its intrinsic complexity. The first objective of this thesis is to study new algorithms and associated architectures to simplify the non-binary decoder. The second objective is to link the decoder task to the synchronisation task. This task is critical when multi-users detection is considered.

More information are available on the QCSP web-site: https://qcsp.univ-ubs.fr

Location: The PhD will be done in the laboratory Lab-STICC (), Université Bretagne Sud, in the town of Lorient (see here for more information.

Salary: The PhD student will receive a salary greater than 2000 euros/month. It also include social security.

Candidate requirement: the candidate should have a **solid background in software and hardware implementation**. Notions of signal processing and some mathematical skills is also a plus. Finally, the candidate should be able to speak and write in English (note: speaking French is not mandatory).

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